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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/348,783	07/07/1999	WEI MA	16556-20	5734
7590	04/30/2004			EXAMINER CAO, DIEM K
JOHN S BEULICK ARMSTRONG TEASDALE LLP ONE METROPOLITAN SQUARE SUITE 2600 ST LOUIS, MO 631022740			ART UNIT 2126	PAPER NUMBER 8

DATE MAILED: 04/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

XU

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/348,783	MA ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Diem K Cao	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 17 February 2004.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-19 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

1. This Office action is in response to the Amendment filed on 2/17/2004.
2. Claims 1-19 remain in the application.

### ***Drawings***

3. The formal drawings were not submitted with the amendment even though Applicant indicated they are submitted. Therefore, the objections to the drawings are maintained.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S. 5,708,838, now refer as Robinson-1) in view of Robinson (U.S. 6,567,837 B1, now refer as Robinson-2).

6. **As to claim 1**, Robinson-1 teaches a host processor (host processor; col. 13, lines 1-8) including a host communication infrastructure configured to provide communication with the host processor (the comms and interface routines; col. 12, line 66- col. 13, line 8), a plurality of class processors (a plurality of object oriented processors 104, 106, 108), and a plurality of

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application program interface modules each configured to provide an interface between the host communication infrastructure and at least one class processor (Each of the object oriented processors includes a Comms interface ... to the host processor 102; col. 7, lines 35-60) wherein each class processor responds to selected data messages on the HCI to perform selected computations (each object oriented processor according to the invention is designed with a specific functionality; col. 14, lines 1-14 and the intelligent message handler ... serviced by it, when the host communicates ... each object oriented processor only responses to messages appropriate to it; col. 8, lines 1-35).

7. However, Robinson-1 does not teach a plurality of class processors each having an associated private localized read/write memory, and each class processor responds to selected data messages on the HCI to perform selected computations utilizing the read/write memory. Robinson-2 teaches a plurality of class processors each having an associated private localized read/write memory (One or more other parts of RAM are ... its functionality; col. 10, lines 11-41), and each class processor responds to selected data messages to perform selected computations utilizing the read/write memory (One or more other parts of RAM are ... its functionality; col. 10, lines 11-41 and the input message ... for named instantiation of the object; col. 5, lines 44-52).

8. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and Robinson-2 because it provides an object oriented processor array that utilizes memory in an efficient manner (col. 4, lines 23-25).

9. Claims 2-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S. 5,708,838, now refer as Robinson-1) in view of Robinson (U.S. 6,567,837 B1, now refer as Robinson-2) further in view of Admitted Prior Art (APA).

10. **As to claim 2,** Robinson-1 does not teach the distributed processing system is integrated onto a single chip substrate. APA teaches the distributed processing system is integrated onto a single chip substrate (on the chip; page 1, lines 15-27). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and APA because it provides powerful computational platforms on a single chip.

11. **As to claim 3,** Robinson-1 teaches each of the plurality of class processors is configured to perform operations on a selected proper subset of application objects (each object oriented processor according to the invention is designed with a specific functionality; col. 14, lines 1-14 and the code for the object oriented processors and the host ... be written as the main; col. 17, lines 62-67).

12. **As to claim 4,** Robinson-1 teaches the processors are configured to reference other class processors, if at all, only through their respective application program interface modules (allow for direct ... generate messages within the object oriented processor; col. 18, lines 1-30), without reference to data structures operated upon by other referenced class processors (and the code for the object oriented processors and the host ... be written as the main; col. 17, lines 62-67).

13. **As to claim 5,** Robinson-1 teaches the plurality of class processors comprise a plurality of classes of class processors (two or more object oriented processors having the same type of task; col. 8, lines 35-38). However, Robinson-1 does not teach at least one of the class processors has an associated protected localized read/write memory accessible only to itself and to at least one other class processor of the same class. Robinson-2 teaches at least one of the class processors has an associated protected localized read/write memory accessible only to itself and to at least one other class processor of the same class (When an object is instantiated ... their allocated RAM in this manner; col. 10, lines 30-35 and the microprocessors 523a-c provide separate processors for each instantiation of an object ... loading software into one of the processors 523a-c; col. 17, line 63 - col. 18, line 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and Robinson-2 because it provides an object oriented processor array with enhanced post-manufacture configurability.

14. **As to claim 6,** Robinson-1 does not teach semi-private busses coupled to the class processors of the same class providing access to the protected localized read/write memory. Robinson-2 teaches a plurality of micro processors are connected in an object oriented processor array (Fig. 9). Obviously, there is a bus in the object-oriented processor array to connect the input processor to plurality of microprocessors.

15. **As to claim 7,** Robinson-1 teaches the plurality of class processors each further comprise

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a special purpose processor (floating point processor; col. 6, lines 45-59). However, Robinson-1 does not teach a special purpose processor coupled to the private localized read/write memory, and public read/write memory, and the public read/write memory is configured to be addressable both to the host processor via the HCI and to the special purpose processor. Robinson-2 teaches a plurality of processors are coupled to the memory (Fig. 1 and col. 7, lines 53-65) wherein the memory includes a public memory (The instantiation of the system object ... which are common to all objects; col. 9, lines 22-39) and a private memory (When an object is instantiated ... of its functionality; col. 10, lines 11-41), the public memory is configured to be addressable to the processor (The first part is the ... the source ID; col. 10, lines 30-36) and the host processor (The system object ... common to all objects; col. 9, lines 32-39 and the host may send global configurations to the system object ... instantiate this particular object; col. 12, lines 29-49). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and Robinson-2 because it provides a method to utilize memory in an efficient manner.

16. **As to claim 8,** Robinson-1 teaches the plurality of class processors comprise a plurality of classes of class processors (the first object oriented processor 104, the second processor 106, the third processor 108; col. 7, line 62 – col. 8, line 27 and there are two or more object oriented processors having the same type of task; col. 8, lines 35-38 and the code for each object oriented processor would be written as a class; col. 17, lines 62-67), and the distributed processing system is configured to restrict direct data communication between the class processors to data communication between class processors of the same class (generates messages within the object

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oriented processor ... from the host processor; col. 18, lines 1-30 and the object oriented processors communicate with the host processor and with each other via the "comms link" or "comms bus"; col. 20, lines 34-39).

17. **As to claim 9,** Robinson-1 does not teach at least a first class processor and a second class processor of the same class, the first class processor further comprises a protected localized read/write memory, and the first and second class processor are configured so that the protected localized read/write memory of the first class processor is addressable by the second class processor. Robinson-2 teaches at least a first class processor and a second class processor of the same class (active object 23a, 23b; col. 8, lines 9-12 and an object is instantiated by loading software into one of the processors 523a, etc; col. 18, lines 1-2), the first class processor further comprises a protected localized read/write memory (the first part is ... the source ID; col. 10, lines 30-34), and the first and second class processor are configured so that the protected localized read/write memory of the first class processor is addressable by the second class processor (This first part is common to all object ... one or more other parts of RAM are arranged for private data used by the instantiated object; col. 10, lines 34-41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and Robinson-2 because it provides a method to utilize memory in an efficient manner.

18. **As to claim 10,** Robinson-1 does not teach at least one class processor further comprises a public localized read/write memory and the class processor having the public localized

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read/write memory is configured so that the public localized read/write memory is addressable by the host processor. Robinson-2 teaches at least one class processor further comprises a public localized read/write memory and the class processor having the public localized read/write memory is configured so that the public localized read/write memory is addressable by the host processor (The system object ... common to all objects; col. 9, lines 32-39 and the host may send global configurations to the system object ... instantiate this particular object; col. 12, lines 29-49).

19. **As to claim 11**, Robinson-1 does not teach the class processors are controlled and activated by the host processor. Robinson-2 teaches the class processors are controlled and activated by the host processor (In response to a high level command from a host processor ... to instantiate itself in RAM; col. 5, lines 6-9).

20. **As to claim 12**, Robinson-1 does not teach the class processors are controlled and activated by the host processor exclusively via the application program interface modules. Robinson-2 teaches the class processors are controlled and activated by the host processor exclusively via the application program interface modules (In response to a high level command from a host processor ... to instantiate itself in RAM; col. 5, lines 6-9).

21. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S. 5,708,838, now referred to as Robinson-1) in view of Patel et al. (U.S. 5,513,369).

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22. **As to claim 13,** Robinson-1 teaches partitioning the application into functions and data messages (the code for the object oriented processors ... would be written as the main; col. 17, lines 62-67 and distributing processing tasks between a host processor and at least one object oriented processor; col. 4, lines 22-25), configuring a host processor having a host communication infrastructure to pass data messages via the HCI to control the application (the comms and interface routines; col. 12, line 66- col. 13, line 8), configuring a plurality of class processors to compute the functions into which the application is partitioned in response to the data messages (a plurality of object oriented processors 104, 106, 108; col. 7, lines 35-60 and each object oriented processor according to the invention is designed with a specific functionality; col. 14, lines 1-14), and interconnecting the class processors to the host processor via application program interface modules (Each of the object oriented processors includes a Comms interface ... to the host processor 102; col. 7, lines 35-60).

23. However, Robinson-1 does not teach interconnecting the class processors to the host processor in a star configuration. Patel teaches interconnecting the class processors to the host processor in a star configuration (Each subsystem includes a plurality of processors 14 ... of each subsystem; col. 3, lines 15-18).

24. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and Patel because it provides a new and useful method for interconnecting processors within a distributed data processing system (col. 2, lines 1-3).

25. Claims 14 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S. 5,708,838, now refer as Robinson-1) in view of Patel et al. (U.S. 5,513,369) further in view of Robinson (U.S. 6,567,837 B1, now refer as Robinson-2).

26. **As to claim 14**, Robinson-1 does not teach at least one class processor comprises a private localized read/write memory, and protecting the private localized read/write memory from being read and from being altered by the host processor and the other class processors, except in response to predefined data messages sent to an application program interface module instructing the class processor to execute a function. Robinson-2 teaches at least one class processor comprises a private localized read/write memory (one or more parts of Ram are arranged for private data; col. 10, lines 11-41), and protecting the private localized read/write memory from being read and from being altered by the host processor and the other class processors (One or more other parts of RAM are ... its functionality; col. 10, lines 11-41), except in response to predefined data messages sent to an application program interface module instructing the class processor to execute a function (One or more other parts of RAM are ... its functionality; col. 10, lines 11-41 and the input message ... for named instantiation of the object; col. 5, lines 44-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and Robinson-2 because it provides an object oriented processor array that utilizes memory in an efficient manner (col. 4, lines 23-25).

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27. **As to claim 17,** Robinson-1 does not explicitly teach wherein partitioning the application into functions and data messages comprises the steps of identifying signals as objects and transforms of signals as functions, grouping functions into groups of related functions independent of others of the groups of related functions, and configuring each of the plurality of class processors to compute a group of related functions to reduce communication between class processors and the host processor. Robinson-1 teaches an object oriented processor with speech processing functionality, wherein the functionality layer is implemented by the analog and digital converter, and the analog audio signals is converted into digital signals (col. 16, lines 1-36), Robinson-1 further teaches the code for each object oriented processor would be written as class (col. 17, lines 62-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve the system of Robinson-1 because in object oriented programming language, noun could be implemented as object and verb could be implemented as function.

28. **As to claim 18,** Robinson-1 does not explicitly teach grouping functions into groups of related functions that have independent data structures, and configuring each of the plurality of data structures comprises configuring each of the class processors to have no knowledge of data structures in other class processors and to communicate with other class processors only through their respective application programming interface modules. However, Robinson-1 teaches the code for each object-oriented processor would be written as class (col. 17, lines 62-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made the system of Robinson-1 would have implemented the above because it bases on the fundamental of

object oriented programming language.

29. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S. 5,708,838, now refer as Robinson-1) in view of Robinson (U.S. 6,567,837 B1, now refer as Robinson-2) and Patel et al. (U.S. 5,513,369) further in view of Admitted Prior Art (APA).

30. **As to claim 15**, Robinson-1 does not teach forming the distributed processing system on an integrated circuit chip, and locating class processors for executing functions most frequently required by the application most physically proximate the host processor on the integrated circuit chip. APA teaches the distributed processing system is integrated onto a single chip substrate (on the chip; page 1, lines 15-27), and interconnecting the processors via at least one member of the group of interconnections consisting of virtual socket interfaces, communication backbones, interface buses (page 1, lines 20-26). It would have been obvious to apply the teaching of APA to the system of Robinson-1 because it provides powerful computational platforms on a single chip, and since the processors are connected via buses, it would have been obvious to put the processor that is most frequently required by the host closer to the host because it provides less time for communication.

31. **As to claim 16**, Robinson-1 teaches the code for each object oriented processor would be written as class (col. 17, lines 62-67), each object oriented processor according to the invention is designed with a specific functionality (col. 14, lines 1-14), and two or more object oriented

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processors having the same type of task (col. 8, lines 35-38). However, Robinson-1 does not teach grouping functions into groups of related functions, interconnecting a group of class processors for executing a group of related functions, the group of class processors including the class processor having the protected read/write memory so that the protected read/write memory is accessible to a plurality of the group of class processors, and protecting the protected read/write memory from being read and from being altered by the host processor and other class processors not in the group of class processors. Robinson-2 teaches at least one of the class processors has an associated protected localized read/write memory accessible only to itself and to at least one other class processor of the same class (When an object is instantiated ... their allocated RAM in this manner; col. 10, lines 30-35 and the microprocessors 523a-c provide separate processors for each instantiation of an object ... loading software into one of the processors 523a-c; col. 17, line 63 - col. 18, line 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and Robinson-2 because it provides an object oriented processor array with enhanced post-manufacture configurability.

32. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S. 5,708,838, now refer as Robinson-1) in view of Patel et al. (U.S. 5,513,369) further in view of Admitted Prior Art (APA).

33. **As to claim 19**, Robinson-1 as modified does not teach wherein interconnecting the class processors to the host processor via application program interface modules in a star configuration

comprises the step of interconnecting the class processors to the host processor via at least one member of the group of interconnections consisting of virtual socket interfaces, I/O port data exchange interfaces, memory mapped dual port random access memory banks, stacks, and first-in-first-out memory. APA teaches the step of interconnecting the processors via at least one member of the group of interconnections consisting of virtual socket interfaces, communication backbones, and interface buses (page 1, lines 20-26). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Robinson-1 and APA because it provides a unified environment.

***Response to Arguments***

34. Applicant's arguments filed 2/17/2004 have been fully considered but they are not persuasive.

35. As to Applicant's arguments (pages 10-11) regarding Robinson '837 does not teach class processors each having an associated private localized read/write memory, examiner respectfully disagrees because Robinson '837 teaches a class processor having multiple objects carry out the functionality of the processor, each object having a private localized read/write memory (col. 10, lines 10-41), Applicant simply argues without giving reason why the cited passages does not teach the limitation. Applicant further argues that the combination of Robinson '838 and Robinson '837 does not teach "a plurality of application program interface modules ... their respective read/write memory), again, Applicant only argues without explaining why the cited passages from two references fail to teach the limitation (see rejection of claim 1 above).

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Therefore, the combination of Robinson '838 and Robinson '837 teaches all the limitations of claim 1.

36. As to Applicant's arguments (pages 11-12) regarding the combination of Robinson '838 and Robinson '837 fails to teach a plurality of classes of class processors with associated protected localized read/write memory, semi-private busses coupling class processors of the same class, and class processors which include private, protected, and public localized read/write memory, examiner respectfully disagree because examiner clearly pointed out in the previous Office action (again in this Office action) the teaching of Robinson '838 and Robinson '837. As before, Applicant simply argues without giving any reason why the cited passages does not teach the claimed limitation. Therefore, the arguments are not persuasive.

37. As to Applicant's arguments (page 13) regarding Robinson '838 in view of Patel does not teach "configuring a plurality ... to the data messages", Robinson '838 teaches pre-partitioned object-oriented processors, and Patel does not teach class processing, examiner respectfully disagrees because the application in the context of the claimed invention is a physical layer processor for communication (page 4, lines 12-16). Robinson '838 teaches selecting pre-programmed object oriented processor to create and processor application for the system, wherein each object oriented processor is selected to carry out certain functionalities, and the host processor is written as main function, and the code for object-oriented processors are written as classes. Further, the class processors are taught by Robinson '838, not Patel, wherein Patel's

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reference is used to show a star configuration can be used to connect multiple processors in the system. Thus, the combination of Robinson '838 and Patel teaches all the claimed limitations.

38. As to Applicant's arguments regarding the Examiner has not pointed to any prior art that teaches or suggests to combine the references, other than Applicant's own teaching, examiner respectfully disagree because the motivation to combine does not necessary come from the reference but could be from one of ordinary skill in the art, most of the motivations used in the Office action are from the reference itself, the system of Robinson '838 and Robinson '837 are related, i.e. from the same structure as set forth in the reference of Robinson '837, and Robinson '838 clearly pointed out any configuration could be used, therefore, one of ordinary skill in the art could apply the teaching of Patel to Robinson '838 based on its suggestion. Therefore, the arguments are not persuasive.

### *Conclusion*

39. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Diem K Cao whose telephone number is (703) 305-5220. The examiner can normally be reached on Monday - Thursday, 9:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (703) 305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Any response to this action should be mailed to:**

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